REMARKS

These remarks are in reply to the Office Action dated March 27, 2006 (Paper No./Mail Date 20060317).

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter as required by 37 C.F.R. §1.75(d)(1) and MPEP §608.01(o). In addition, Claims 1-20 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Pat. to Lewis, et al.[1] ("Lewis"). Claims 1-20 have been amended. Applicant respectively traverses the rejections.

Objection

The specification has been amended. This amendment does not constitute new matter. See MPEP 2163.06. Applicant respectfully submits that the objection as to lack of antecedent basis be withdrawn.

Claim Rejections

The present application discloses:

> "if the upper byte UB_2 of the second address is equal to the upper byte UB_1 . . . there is no need to transmit the byte UB_2 . . . the CPU . . . recognizes that it need only transmit the lower byte LB_2, thereby saving an address cycle . . . The logic circuit 42 advantageously recognizes this determination by the CPU *without the need for providing an additional line between the CPU and the memory device.*"[2]

In contrast, Lewis discloses providing two additional signals between each bus master and the memory controller:

> "The present invention is a system and method to reduce the memory read data latency . . . *Adding a point to point cache line address and a previous address valid signal from each bus master to the memory controller* allows the controller to start fetching the data at least three cycles earlier than in conventional methods."[3]

Amended claim 1 is illustrative. Amended claim 1 comprises:

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[1] U.S. Pat. No. 5,913,231
[2] Application, page 7, line 12 – page 8, line 2 (emphasis added).
[3] Lewis, column 3, lines 15-23 (emphasis added).

> "determining that a first condition is true, the first condition being *that an address of a first location* in a memory space *has been transmitted on a bus*, the address of the first location including at least one first part and a second part;
>
> determining that a second condition is true, the second condition being *that at least one first part of an address of a second location* in the memory space *has been transmitted on the bus* in a particular address cycle." (emphasis added.)

In comparison, the Lewis reference discloses that "preferably, the portion of the second address which is provided is a cache line address for the second request."[4] Lewis states: "processor 102c sends a cache line address and a previous address valid signal to memory controller 106 via step 414."[5] In addition, "FIG. 6*b* shows a signal diagram corresponding to steps 400 and 414-418 of FIG. 5."[6] Referring to Lewis Figures 6*a* and 6*b*, it can be seen that the "Cache Line Address" and the "Bus Address" are distinct from one another. Accordingly, Lewis fails to disclose transmitting part of an address for a second location on the same bus that is used to transmit the address for a first location. Thus, Lewis does not disclose each and every element of independent claim 1. Amended claims 2-6, and 19 depend from claim 1 and are not anticipated by Lewis for the same reason that claim 1 is not anticipated.

As mentioned, claim 1 is illustrative. Just as Lewis does not disclose each and every element of claim 1, it fails to disclose each and every element of the independent claim 13. Amended claim 13 comprises a unit that makes determinations similar to those quoted above from claim 1. In addition, amended claims 12-17 depend from claim 13 and are not anticipated for the same reason the claim 13 is not anticipated.

Amended claim 7 comprises a unit that:

> ". . . in response to *transmission of the first data on the bus* in a next data cycle, the first data being at least one first part of *an address of a first location* in a memory space;
>
> . . . in response to a *transmission of the second data on the bus* in a next data cycle, the second data being a second part of *the address of the first location* in the memory space;

[4] Lewis, col. 3, lines 32-33.
[5] Lewis, col. 3, line 67 - col.4, lines 1-3.
[6] Lewis, col. 4, lines 26-27.

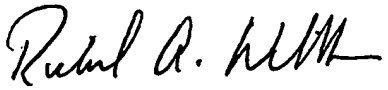
> stores third data in the first register, in response to *transmission of third data on the bus*, . . . the third data being at least one first part of *an address of a second location* in the memory space."

However, as mentioned, Lewis fails to disclose transmitting part of an address for a second location on the same bus that is used to transmit the address for a first location. Accordingly, Lewis does not disclose each and every element of independent claim 7. Amended claims 8-12, and 20 depend from claim 7 and are not anticipated by Lewis for the same reason that claim 1 is not anticipated.

Conclusion

Accordingly, claims 1-20 are in condition for allowance. Applicant respectively requests that claims 1-20 be allowed, and this application be passed to issue.

Respectfully submitted,



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